semiconductor device **500**. An output of the control circuit **520** is electrically connected to the control electrode CTR of the semiconductor element **510**. A further output of the control circuit **520** may be electrically connected to the gate electrode GA, if applicable. According to other embodiments, the gate electrode GA may be directly connected to the gate terminal G. The control circuit **520** may be electrically connected to at least one of the load terminals, for example to an emitter terminal E, of the semiconductor device **500**.

The control circuit **520** generates a desaturation signal applied to the control electrode CTR from a signal applied to the gate terminal G.

The semiconductor device **500** may be arranged to be operated in combination with a new type of gate drivers delivering a desaturation signal, wherein the new type of drivers generate the gate signal in advance with respect to conventional gate drivers. The control circuit **520** may apply the advanced gate signal to the control electrode CTR and a delayed gate signal to the gate electrode GA.

According to another embodiment the semiconductor device **500** is arranged as a one-to-one replacement for existing semiconductor switches in combination with existing gate drivers providing a timed desaturation signal on the gate line. The control circuit **520** (i) extends an applied desaturation pulse such that a time lag between the end of the desaturation pulse of a conventional IGBT driver and the gate signal for driving the controllable switching element **510** into the forward conductive mode is reduced by at least 10%, 50% or is completely omitted and (ii) prompts the gate-on voltage for the forward conductive mode of the switching element **510** to gradually decay below the threshold voltage of the semiconductor element **510** within a predetermined threshold time. With respect to the signal applied to the gate electrode Ga, the control circuit **520** may be transparent.

FIG. **6**B schematically shows the step signal response U_{CTR} of the control circuit **520**. U_{CTR} follows with only little delay the leading edge of U_G and falls below a threshold UTH above which the recombination regions are connected to the drift zone at the predetermined threshold time t_{th}.

FIG. **6**C schematically shows the square wave response of the control circuit **520**. The desaturation pulse length t1 is shorter than the threshold time t_{th}. The control circuit **520** delays the trailing edge of the desaturation pulse such that U_{CTR} falls below U_{th} at a defined delay t2−t1.

Numerous gate drivers are available at present that provide a defined desaturation pulse in advance of a gate signal controlling the forward conductive mode of power switching element such as power MOSFETs and IGBTs. The control circuit **520** facilitates a one-to-one replacement of conventional power switching devices or power semiconductor diodes with power switching devices or semiconductor diodes with switchable recombination regions as described above.

The control circuit **520** may be or may include a differentiator or a high pass. According to an embodiment the control circuit **520** includes exclusively passive elements or exclusively passive elements and semiconductor diodes and is devoid of semiconductor switches.

FIG. **7**A shows an embodiment of the control circuit **520** based on a serial arrangement of a capacitor C**1** and a diode D**1** forming a high pass.

FIG. **7**B shows a further embodiment with the high pass of FIG. **7**A and a resistor termination R**2** between the control input CTR of the switchable semiconductor element and the emitter terminal E.

FIG. **7**C shows a schematic equivalent circuit diagram of the semiconductor device **500** between the terminals G and E using the control circuit **520** of FIG. **7**B.

FIG. **8**A shows the square signal response and FIG. **8**B the step signal response of the control circuit of FIG. **7**C with R**1**=10Ω, R**2**=400Ω, CSOX=CGOX=10 nF and C**1**=40 nF.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that a variety of alternate and/or equivalent implementations may be substituted for the specific embodiments shown and described without departing from the scope of the present invention. This application is intended to cover any adaptations or variations of the specific embodiments discussed herein. Therefore, it is intended that this invention be limited only by the claims and the equivalents thereof.

What is claimed is:

1. A semiconductor device, comprising:
a drift zone in a semiconductor body;
a charge-carrier transfer region forming a pn junction with the drift zone in the semiconductor body and directly electrically connected to a first load electrode;
a recombination region; and
a control structure comprising a connection region of a conductivity type of the drift zone, the connection region being electrically insulated from the first load electrode and directly adjoining the recombination region, wherein the control structure is configured to electrically connect the recombination region to the drift zone during a desaturation cycle and to disconnect the recombination region from the drift zone outside of the desaturation cycle.

2. The semiconductor device of claim **1**, wherein
the recombination region is arranged to float outside the desaturation cycle.

3. The semiconductor device of claim **1**, wherein
a surface recombination velocity of the recombination region is at least 0.5% of a saturation velocity of charge carriers in the semiconductor body.

4. The semiconductor device of claim **1**, wherein
a surface recombination velocity of the recombination region is at least 5×10^4 cm/s.

5. The semiconductor device of claim **1**, wherein:
the control structure comprises a separation region of a conductivity type of the charge-carrier transfer region;
the separation region separates the recombination region from the drift zone; and
the control structure is configured to form, during the desaturation cycle, an inversion channel of minority charge carriers that temporarily connects the recombination region with the drift zone.

6. The semiconductor device of claim **5**, wherein:
the control structure further comprises a control electrode and a control dielectric separating the control electrode from the separation region; and
the desaturation cycle is controllable by a variation of a control voltage applied to the control electrode.

7. The semiconductor device of claim **6**, wherein
the control electrode and the control dielectric are arranged in a trench structure extending between the charge-carrier transfer region and the separation region from the first surface down to at least the drift zone.

8. The semiconductor device of claim **1**, wherein:
the semiconductor device is a controlled diode; and
the charge-carrier transfer region is electrically connected to a load electrode.